edaTrend DATE07

Collected EDA essentials in industry and business

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DATE07
April 16-20, 2007
Nice, France

About edaTrend DATE07

The "edaTrend DATE07" report summarizes the important topics and trends from the 10th "Design Automation and Test" Conference (DATE) in Nice, France. Due to the huge amount of information presented at DATE, the "edaTrend DATE07" report focuses on the conference's top events, such as its keynotes and panel discussions. Here, you will find many essential details and personal impressions gathered on site by our team of editors.

The "edaTrend DATE07" report is divided into several sections: The first section contains general information about DATE, the second discusses the technical program (and the panel sessions in particular), and the third focuses on the panel sessions in the Exhibition Theatre, but also includes some impressions from the exhibition. One very special highlight of Section 3 is an interview with Chris Rowen, CEO and President of Tensilica, who spoke exclusively with edacentrum on the subject of ESL and configurable processors.

Fig. 1: DATE07 was held at Acropolis, Nice, France

Fig. 2: The beach of Nice

Imprint

„edaTrend DATE07" was published in June 2007 by edacentrum GmbH.

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30167 Hanover, Germany

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Printed by Druckerei Hartmann GmbH, Germany

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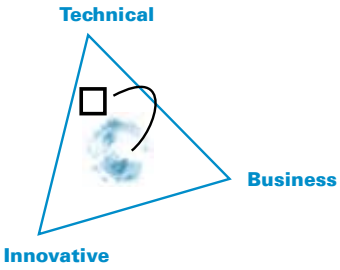

Trading energy for flexibility with customizable processors

8.6 EMBEDDED TUTORIAL/PANEL –
The future of customizable processors:
Are we there yet? –
Thu, 0830 - 1000, Erato, Level 3

Keywords: MPSoC, ESL, configurable, extendible, processor, software, compiler, heterogeneous, multi-processor

Abstract

Customizable processors are being used increasingly in SoC designs. During the past few years, they have proven to be a good way to solve the conflicting flexibility and performance requirements in embedded systems design. While their usefulness has been demonstrated in a wide range of products, this panel addressed the challenges that remain.

Panelists

- P. Paulin, STMicroelectronics (Moderator)
- L. Pozzi, Lugano U (Tutorial Speaker)
- C. Rowen, Tensilica
- H. Meyr, Aachen U / CoWare
- N. Topham, ARC
- N. Wehn, Kaiserslautern U
- J. M. Moutin, STMicroelectronics
- P. Young, Nemerix

Energy vs. Flexibility

Although it started at 8:30 a.m. on the day after the DATE event, a large audience attended this panel discussion. The excellent tutorial speaker, Laura Pozzi, and the experienced panel moderator, Pierre Paulin, made it worth getting up early.

The future of customizable cores is safe. This became obvious within just a few minutes.

Small changes to the instruction set architecture (ISA) of a generic RISC can have a significant influence on performance and power. If, for example, the inner loop of a computation-intensive data processing algorithm can be sped up by supplying the designer with specialized instructions, a performance improvement of 5 to 10 times the level of the overall algorithm is not unusual.

On the other hand, vectorization of data processing can lead to a decreased clock frequency which, in turn, means less power consumption.

Fig. 1: Moderator P Paulin from ST Microelectronics

"If your application allows you to use a RISC with extensions, you should do so."
Heinrich Meyr, University of Aachen / Coware

The question, however, is if this should be done semi-automatically with manually extended and configured RISC processor core templates or with fully-customized processors. Both methods require a new mindset on the part of the hardware designer, who now must have a clear understanding of the software algorithm running on the core. Furthermore, good communication between the software designer optimizing the algorithm and the hardware designer providing the means for it is a must.

"Automation is the low-hanging fruit."
Chris Rowen, CEO of Tensilica

The question in which way this is done, however, is associated with significant commercial impact.

Overall impression

★★★★★

Excellent speaker / moderator, good presentations, hot topic

If area and/or power are high-priority issues for the design in question, a fully customizable processor design approach might be the best choice. These implementations, therefore, tend to be targeted to one specific application.

If the time-to-market window is most critical, a more highly automated method using a processor template approach is probably faster for implementation and verification. A good approach here is to not only target a specific application, but also make the processor generic for a specific domain of applications. This additionally opens up the door for reuse of designs, late specification changes, and application software updates.

Another important aspect is royalties. The market segment that a company is addressing might force it to build an in-house, royalty-free core so that the end product fits into a certain range of production costs. The use of a configurable processor template – which currently always involves royalties – might not be an option here.

One big disadvantage of fully customizable cores, however, was missing during the discussion: verification of a processor is non-trivial and can be considered a highly sophisticated task. This comes for free when you use processor templates.

No matter what strategy is used, a design with customizable processors will only be accepted in the future if automated software tool-chain generation is provided. Then the question is not whether or not you should use configurable cores, but what to watch out for when you do.

For this reason, Phil Young of Nemerix strongly recommended that HW/Software interactions should be simplified in order not to loose performance at the interface. Furthermore, the impact of multi-threaded applications and pre-emptive context saving must be taken care of. Finally, data-structure ordering has a huge impact on accelerated hardware. Or simply speaking: Ultimately, load/store is limiting data processing systems.

"Don't leave the architecture entirely to a tool."

Phil Young, Chief Scientist, Nemerix

There is also a trade-off between algorithm vs. implementation optimization. Since experts know the applications best, they should not leave the architecture entirely to a tool. Automation processes are not able to replace the designers' knowledge of applications and algorithms.

Fig. 1: Chris Rowen from Tensilica, a panelist full of engagement

So will we see heterogeneous or homogeneous multi-processor systems in the future? The panel agreed that fully homogeneous MP systems will not be mainstream for some time. A mixture of both, however (where, for example, a main CPU oversees a set of homogeneous data processing processor cores), is already available in some products today. Probably the biggest future challenge is the interaction of cores and the automation of partitioning software on multi-processor systems-on-chip (MPSoC).

Conclusion

Customizable, configurable cores already reach a significant volume in shipped units today. So are we there yet? The answer is probably yes.

However choosing the right approach, i.e. a fully customizable core or an extendable RISC, depends significantly on the application.

A design with configurable and extendable cores speeds up the design process and offers a considerable advantage in verification, since the processor comes as a pre-verified piece of IP.

The designer's knowledge of the application can never be replaced. So for very specific applications, fully customizable processors are probably the best option.

Or to quote Prof. Meyr: "It's not about design automation, it's about design efficiency in cost."

Author

Peter Neumann, edacentrum

About us

edacentrum and edaTrend authors

The edacentrum is an independent organization dedicated to the promotion of research and development in the area of electronic design automation (EDA). Its main role is to initiate, evaluate and supervise industry driven EDA R&D projects and to provide individual services in the EDA sector. Further by encouraging cluster research projects and EDA networks, it bundles and reinforces the EDA expertise of universities and research institutes.

The edacentrum provides individual services in the EDA sector, including consulting, project management, the organization of trainings, workshops and networking events and provides a communication platform to the EDA community. The edacentrum actively engages in public relations in order to sensitize higher management levels, the public and the political arena about the central importance of design automation in solving the system and silicon complexity problems in microelectronics.

The edacentrum consists of an association (edacentrum e.V.) and a company (edacentrum GmbH). The association operates on behalf of its members and the projects supported by it and actively engages in public relations for EDA. The company provides individual services in the EDA sector. At present more than 50 companies are member of the edacentrum e.V. The association is open to all persons and legal entities.

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