edaTrend DATE08

Collected EDA essentials in industry and business

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DATE08
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About edaTrend DATE08

The “edaTrend DATE08” report summarizes the significant topics and trends at the 11th Design Automation and Test Conference (DATE) in Munich, Germany. Because the DATE generates a huge amount of information, the “edaTrend DATE08” report focuses on the essentials – the top events, such as keynotes and panel discussions. The report was compiled by edacentrum representatives, who personally attended these sessions.

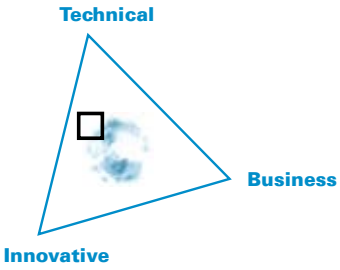
The “edaTrend DATE08” report is divided into several sections: the first section contains general information about DATE; the second section discusses the technical program (and the panel sessions in particular), and the third covers some panel sessions in the Exhibition Theatre, but also includes some impressions from the exhibition. Section four consists of an interview with Alberto Sangiovanni-Vincentelli, University of California, Berkeley. “edaTrend DATE08” concludes with a short commentary and the list of contributors.

Fig. 1: Munich, Germany, place of the Design, Automation & Test in Europe (DATE)

Fig. 2: The International Congress Centre Munich (ICM) – venue of DATE08 (Copyright by Messe München GmbH)

Content

Quo Vadis Electronic Chip Design?



Huge Impact of System-Level Design on Society

Plenary Keynote, Giovanni De Micheli
Designing Micro/Nano Systems for a Safer and Healthier Tomorrow
March 11th 2008

Keywords: lab on chip, bio-analysis, wireless sensor networks, heterogeneous systems, interconnect technologies, 3D integration

Abstract

The ongoing scaling and hybridisation of manufacturing technologies enables us to attain unprecedented levels of performance, as well as to integrate electronic and fluidic circuits with sensors and actuators. Smart micro/nano systems will be the building blocks of wearable and ambient systems, that gather and integrate heterogeneous data in real time and operate and communicate in a wireless and ultra low power mode. This keynote discussed how these systems can foster a revolution in health and environmental management, with the objective of improving security and quality of life.

Furthermore, a large market of components and systems, a renewed perspective for electronic design and manufacturing companies will be created by these applications.

Giovanni De Micheli, EPF Lausanne

Giovanni De Micheli is Professor and Director of the Institute of Electrical Engineering and of the Integrated Systems Centre at EPF Lausanne, Switzerland. He also chairs the Scientific Committee of CSEM, Neuchâtel, Switzerland. Previously, he was Professor of Electrical Engineering at Stanford University. He holds a Nuclear Engineering degree (Politecnico di Milano, 1979), and M.S. and Ph.D. degrees in Electrical Engineering and Computer Science (University of California at Berkeley, 1980 and 1983).

Giovanni De Micheli discussed EDA in the context of the major challenges facing our society. So, for him the question "Quo vadis, electronic chip design?" cannot be separated from the question "Can we have a deeper impact on society?" Electronics has come a long way from the transistor radio of 50 years ago to today's notebooks and mobile phones. Electronic Design

Fig. 1: Giovanni De Micheli

Automation (EDA) has provided us with the enabling chip design technology, but now needs to be repositioned as a central system engineering task. Broadening its scope can create huge value that will affect everyday life.

Multi-processor systems, new fabrication technologies beyond CMOS, new computational structures and new communication structures will spark a myriad of new product and application ideas – ideas that require ultra low power, high reliability and high performance. But a central question remains to be answered:

"How do we design them?"
Giovanni De Micheli

3D network-on-chip (NoC) designs enabled by new packaging technology with 3D integration, and the heterogeneous integration of electrical

Overall impression

★★★★★

The keynote presented a fascinating road ahead with many challenges and rewards, EDA will be a key enabler.

and mechanical components, will provide lots of opportunities for new products. But there are difficult challenges such as the development of effective, correct and dependable software system failure must be avoided.

For De Micheli, EDA is the key enabling technology. Its commercial value stems from the systems aspect. EDA needs evolution, for example, in system-level design technology, but also needs to take a bigger perspective in order to master complex multivariate systems and address all aspects of embedded systems design.

"We have to think on a bigger scale now, then we can push forward society and the economy!"
Giovanni De Micheli

As an example, De Micheli presented Lab-on-Chip technology, which performs in-field biochemical tests. It could revolutionize medical care. It will, however, require a broad range of technical developments, ranging from fully integrated sensing techniques to data mining and interpretation.

Bio-analysis and synthesis is a second example of how design automation tools and methods can push further advances. Bio-analysis enables us to understand biological mechanisms and to comprehend the full value of the 'omics' genomics, proteinomics, and so on. Synthesis enables us to modify and/or create new treatments, such as medications that alter genetic/metabolic pathways, and new biological components that perform computation. Here, design automation is in its infancy even basic elements such as libraries have yet to be created.

De Micheli highlighted interconnect technologies as another example of bigger thinking. Forewarning of natural disasters such as the Asian Tsunami could save many lives. The requisite environmental monitoring would require the collection and analysis of massive amounts of data. A distributed intelligence approach with wireless sensor networks could do the job.

De Micheli discussed how electronics will shape the way we interact with the environment, physically as well as socially. Driver assistance systems in the car and bionic eye implants are examples, but also the vision of a virtual DATE 2058 conference, where we let our avatars attend in our place.

De Micheli concluded by calling for a partnership between IEEE and the United Nations in order to identify technologies for the benefit of all countries and people. And he desired an ethical objective that can raise enthusiasm among engineers.

Background: nano-tera program

This Swiss program is an example of the kind of initiative that De Micheli called for. It focuses on the research, design and engineering of complex (tera-scale) systems and networks to monitor and connect humans and/or the environment. The program researches micro/nano-technologies and their application to distributed, networked embedded system design. [1]

Summary

De Micheli described some of the methodological advances and technological changes necessary to designing micro/nano systems for a safer and healthier tomorrow. Multi-processor systems, new fabrication technologies, and new computational and communications paradigms will revolutionize our lives from safety at a global level to medical care at a personal level.

This requires "big picture" thinking in the development of system-level design – its extension to mixed electronics and mechanical design and its expansion to encompass biological systems.

And De Micheli believes that it also requires international co-operation.

Commentary

The keynote presented a fascinating road ahead with many challenges and rewards. It showed that expanding our horizons is key to scientific viability and commercial profitability. Heterogeneous hardware design and a corresponding software infrastructure are needed for product and system design. System-level design technologies are crucial for system conception, design and management. This will lead us far beyond classical silicon chip design, and the system and service perspective will yield scientific and financial benefits. With this keynote, De Micheli made his contribution to raising enthusiasm among engineers. Our society strongly needs this.

Sources

[1] http://www.nano-tera.ch

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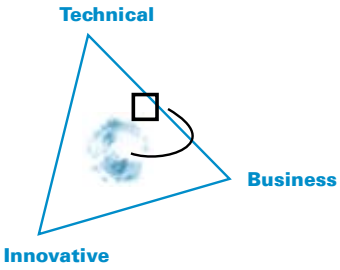
Jürgen Haase, edacentrum

Market Niche or Holy Grail?



Are Virtual Platforms Restricted to Early Software Development?

X7 Exhibition Theatre Panel Session
Virtual Platforms: ESL Hype or Killer App?
March 12th 2008

Keywords: Virtual Platform, Virtual Prototype, Virtual Model, ESL

Abstract

"Virtual Platform" has been the ESL buzzword for the last two years. Virtual platforms hold the promise of enabling early HW/SW integration, architectural exploration, and full system validation. But are they actually being deployed? And are they achieving the benefits envisioned by their proponents?

The panel, including representatives from semiconductor and system houses, tool providers, IP providers, and hardware emulation providers discussed whether virtual platforms can be used throughout the development life-cycle, whether companies already do it, and whether it makes sense at all. They also touched upon the related business issues.

Panelists

- W. Rosenstiel, edacentrum e.V., DE (Moderator)
- J. Aldis, TI, FR
- L. Burgun, EVE USA, Inc., FR
- J. Cornish, ARM, UK
- A. Hoffmann, CoWare, US
- J. Kunkel, Synopsys, US

Virtual Platforms

James Aldis got straight to the point. He asserted that the major value of virtual platforms is software development. TI utilizes several software development aids, including emulation, FPGA models, and of course virtual platforms.

Only virtual platforms provide the software development engineers with an entire system platform. It is available early in the design and it can be fast. It has good debug capability, and the price per seat is low.

There are two drawbacks, however. It is very difficult to develop a virtual platform from scratch – it takes time to get it right. And there is a cultural issue – designers drop the virtual platform as soon as first hardware becomes available.

Fig. 1: John Cornish, ARM

"We're not there, yet."

James Aldis, TI

Although TI uses virtual platforms primarily for early software development, Aldis believes that the ultimate benefit will be its use throughout the system development life cycle.

For ARM, the virtual platform is key to enabling customers to develop software and, consequently, to ensuring the widespread use of ARM processors. Model execution speed is important because software developers expect the software to run as fast as possible. Model accuracy can be refined later in the design process, he said.

Overall impression

★★★★☆

Enlightening and entertaining panel

"For software developers, SystemC and TLM are unknowns, and in many ways, don't cares"
John Cornish, ARM

The implementation of the models and the platform itself is not relevant to the software developers who use it, Cornish added. Of course, it is extremely relevant to the model provider, since support of multiple languages is cost-ineffective.

"The deployment of virtual platforms has been held back by the lack of availability of models"
Joachim Kunkel, Synopsys

Joachim Kunkel stressed the economics. There must be a broad market for models to justify the investment. Since only a few developers need and use such models, the return is inadequate. So, the economics is a barrier to model development.

He fully agreed with Cornish's point that virtual platform implementation languages are of great relevance to model developers. Language and modeling standards are necessary to avoid the cost and interoperability problems created by the use of several incompatible languages – as history has demonstrated on many occasions.

Synopsys currently sees requests for complete, turnkey virtual platforms only from some customers. Others want to be in control of the platform and want to create the models and the platform themselves. So here it's the tools that are of interest, he said.

Kunkel observed that there is a trend to use virtual prototypes for hardware architecture evaluation to optimize performance, timing, power, and so on. Virtual platforms are sometimes even

Fig. 2: Joachim Kunkel, Synopsys

Fig. 3: Andreas Hoffmann, CoWare

used to develop software-based functional tests for the RTL implementation. But Kunkel made it quite clear that he sees the primary reason for virtual platform deployment is pre-silicon software development.

Andreas Hoffmann outlined the design trends of the past years. With every switch in the abstraction level, productivity per design engineer increases by 100x (source: VDC). When reaching the RT level, productivity was additionally increased by outsourcing and by the use of IP.

"We at CoWare think that the free lunch is over"
Andreas Hoffmann, CoWare

In order to maintain the productivity pace, Hoffman stated that the development process must now switch to the next level of abstraction.

While the architectural trends in the past have been mostly in hardware, they are now moving to software, with multi-core designs becoming a major issue for software architecture development.

According to VDC, 24% of projects are cancelled due to project slip, 54% of software designs are completed behind schedule, 33% of devices miss functionality/performance, and 80% of the effort is spent correcting errors detected late in the design cycle. The top issues concern architecture and software integration. ESL is addressing the issue, said Hoffman. He cited again the VDC study which estimates that the use of virtual prototyping is expected to almost double in the next two years.

In Hoffmann's view, virtual platforms are a means to easily build systems out of existing models, using existing tools and methodologies to analyze, elaborate and simulate the HW/SW system prior

to silicon availability. But Hoffmann also stressed the importance of virtual platforms to the marketing team. It enables very early engagement with the customer, and can act as a kind of executable contract between the architect, the hardware and the software designer, the verification engineer, and the marketing team.

But not all panelists sang the Song of Songs to virtual platforms. Luc Burgun wondered whether the virtual platform business is a consulting, an IP, or a product business. Burgun also noted the lack of available models. He further questioned the link to implementation.

In his opinion, virtual platforms are useful for system analysis and early software development. In stark contrast to Aldis, he very much doubted its use throughout the development life-cycle. Being the CEO of an emulation company, he stated that true hardware debugging and hardware/software co-design can be undertaken only at the RT level using emulation. Virtual platforms are of value for early software development when no hardware is available.

Kunkel replied that Synopsys has virtual models and they are provided as IP. The models are designed using standard SystemC and work with every ESL tool. So, although model availability has been limited by economics, it is currently improving.

Hoffmann added that without virtual models customers are not completely lost. Model generators such as those provided by Carbon Design Systems can generate fast virtual models of legacy RTL IP that can then be integrated into an existing virtual platform.

An audience member stated that, in his experience, almost all systems are composed of a high

Fig. 4: Luc Burgun, EVE

Fig. 5: James Aldis, Texas Instruments

percentage of existing blocks and a small percentage of newly-designed ones.

Another audience member, Grant Martin, Chief Scientist at Tensilica, remarked on the link to implementation. A synthesizable model would be a terrible model. The structural information would slow down the execution speed significantly. And the design effort would increase.

Aldis agreed, and added that although TI is using behavioral synthesis, this is only for blocks that have little influence on the simulation load of the system design. For processor models, TI makes quite sure that the model is not linked to implementation because this would have an enormous impact on the computation load.

Finally the panel came back to commercial issues. Virtual platform models can be shipped around the world in no time. Model providers therefore have a basic interest in preventing unauthorized replication.

Platform users on the other hand want a simple, straightforward license model. Aldis wants a license model that enables TI to not only ship a platform to TI development engineers worldwide, but also to its worldwide customers. Kunkel replied that Synopsys is listening to customer requirements, which can always be negotiated.

"If we spend a lot of time negotiating the legal terms of a platform, the fact that we can send it around the world in zero time doesn't help us much"
Joachim Kunkel, Synopsys

But models have to be developed, which requires significant investment. This implies that there also has to be a solid license basis to ensure ROI, concluded Cornish.

Summary

This panel discussed the multiple aspects of virtual platforms. ARM, CoWare, and Synopsys evaluated it from the IP and tool provider's side, and requested development standards and solid license models to ensure ROI.

TI gave the customer's view. TI wants easy usability, and provision to customer locations worldwide without bureaucratic legal negotiations with the platform technology provider.

From the technical point of view, Aldis envisioned the deployment of virtual platforms throughout the full life-cycle of a development. This view was questioned by EVE, which sees final software debug as an RTL hardware emulation task.

Commentary

Although many of the statements sound similar to those of last year's DATE, there seems to be momentum in the ESL business. Some technology providers are partnering more and more with adjacent tool and IP vendors in order to deliver the complete solution that customers seek. Other vendors attack the productivity gap with system level model libraries to support virtual platform generation and with tools to enable model generation of legacy RTL.

So, the industry uses virtual platforms. The big question seems to be whether the deployment will be localized, for example on software development, or generalized throughout the development life-cycle. The answer to this question is best provided by users. [1]

Sources

[1] Virtual platforms - a reality check, http://www.scdsource.com/article.php?id=59

Author

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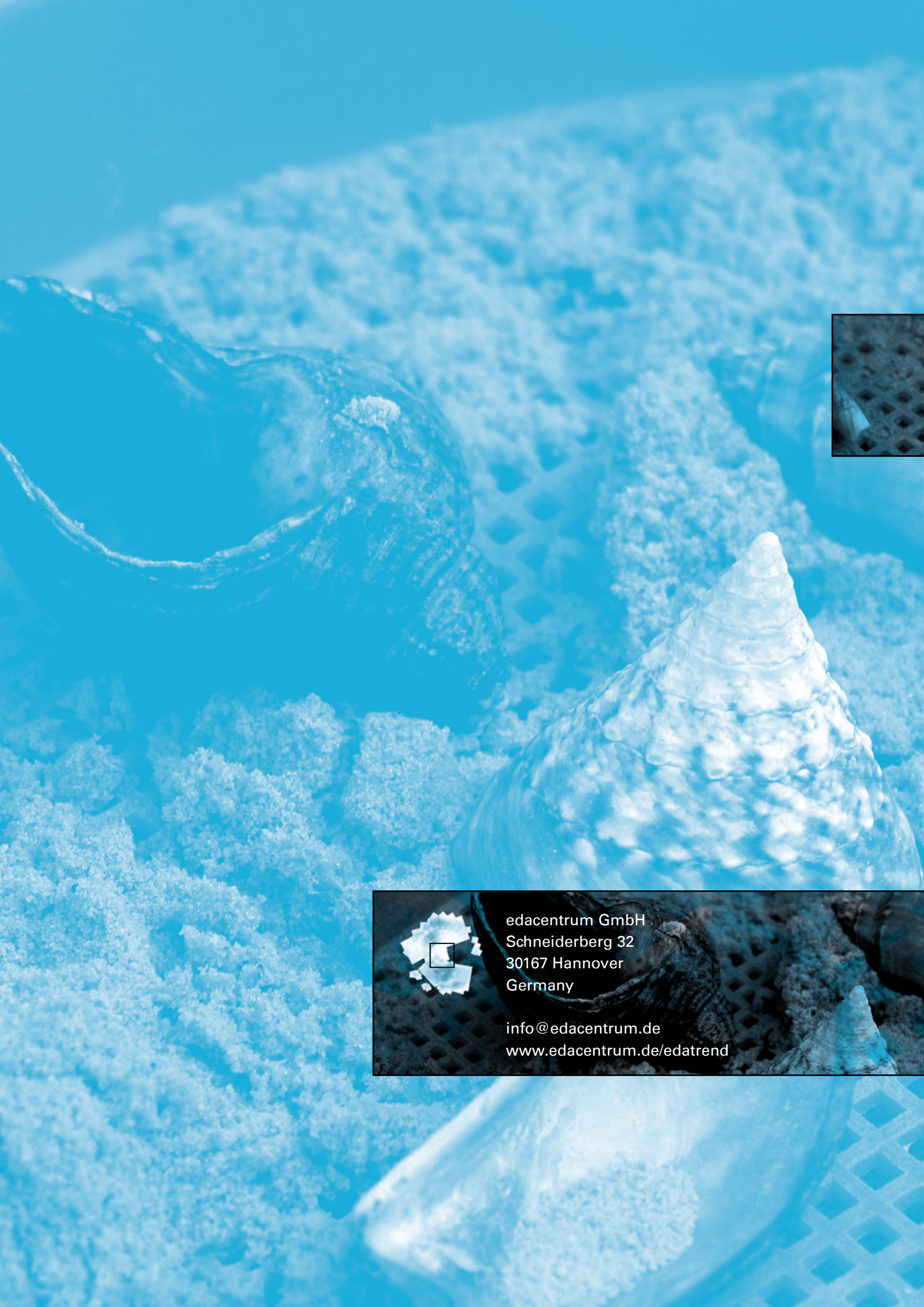

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